Design and FPGA-Implementation of Wave Digital Bandpass Filters with Arbitrary Amplitude Transfer Characteristics

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Abstract— **In most cases, a bandpass filter characteristic is obtained by using a lowpass-to-bandpass frequency transformation on a known lowpass transfer function. This frequency transformation controls the location of passband edges and transfer zero frequencies completely. Using the "Vlach-Chebyshev approximation" [1] however, we are able to specify the (Chebyshev) passband limits directly, together with a free choice of transfer zero locations in the stopband. In this way it is possible to design bandpass transfer functions that cannot be obtained from lowpass functions by a frequency transformation. We think this method to be the only (and not very well known) analytical method to obtain such bandpass characteristics. We show how we designed wave digital realizations from the specification, through a VHDL description and synthesis into a Xilinx FPGA (Virtex-II).**

Keywords— **Bandpass filter design, Wave Digital Filters, FPGA implementation.**

I. Introduction

Usually, a bandpass filter characteristic is obtained by using a lowpass-to-bandpass frequency transformation starting from a normalized and known lowpass transfer function. This frequency transformation determines the location of passband edges and, moreover, transfer zero frequencies, completely. This may impose design compromises, if the transformation would result in a sub optimal characteristic.

Earlier [2], we have shown how to design Chebyshev-like lowpass filters with arbitrary stopband characteristics. With the "Vlach-Chebyshev approximation" [1] we can extent this to a Chebyshev *band*pass with a free choice of transmission zero frequencies in the stopband.

It thus becomes possible to design bandpass transfer functions that cannot be obtained using frequency transformations. We think this method to be the only (and not very well known) analytical method to obtain such bandpass characteristics in the time-continuous domain.

Since we are more interested in time-discrete implementations, we use the well-known bilinear z-transform to change domains. In the following, we describe two wave digital [3] choices for implementation, e.g.

1. a wave digital equivalent of a lossless ladder,
2. a wave digital lattice structure.

Wave digital filters have been proved to be very robust with a guaranteed linear stability even for poles very close to the unit circle.

We show how we designed these realizations from the specification, through a VHDL description through synthesis into a Xilinx FPGA of the Virtex-II family [7]. We will use a 6^{th} order bandpass as an example, where particularly the straightforward design of the lattice implementation is notable. For both choices of implementation, we want to use the 18-bit hardware multipliers that are present in the Virtex-II type of Xilinx FPGAs.

The accuracy of the implemented frequency characteristic is shown by measurement with a spectrum analyzer.

II. The Vlach-Chebyshev Bandpass Approximation Usage

Thanks to the Vlach-Chebyshev approximation, we are able to directly specify the desired passband edges together with the location of the transfer zeros. The

method will find an equiripple approximation for the passband and returns the roots of the denominator polynomial of the transfer function $H(s)$. There are several ways to construct the complete transfer function.

As an example we have chosen a (nearly) symmetrical digital bandpass of order 6. We specify the passband to be between $f/f_s = 0.15 \pm 0.02$ and two transmission zeros at $f/f_s = 0.15 \pm 0.05$ (and at 0 and 0.5) to demonstrate the symmetry and the freedom of choice. The passband ripple is specified to be 1 dB.

Since the Vlach-Chebyshev approximation is derived to work in the time-continuous domain, these specifications have to be prewarped to that domain first through the inverse bilinear transform. Characteristic frequency values resulting from the approximation are shown in figure 2, together with the resulting 6th order transfer function $H(s)$.

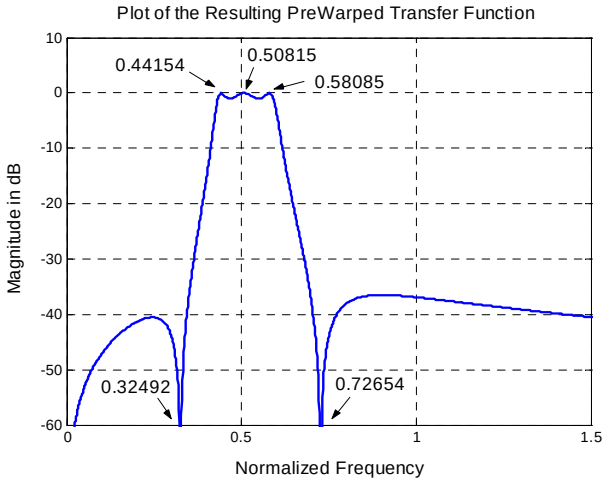


Figure 1. The Vlach-Chebyshev approximation resulting from the specifications.

III. The Resulting Transfer Functions $H(s)$ and $H(z)$.

From the pole locations as given in figure 2 and the zero frequencies, we can write down the transfer function in the s-domain to be of the form

$$H(s) = \frac{s\,(s^4 + a_2 s^2 + a_0)}{\sum_{i=0}^{6} b_i s^i}$$

from which we can –as mentioned before by using the bilinear transformation– derive the transfer function in the z-domain:

$$H(z) = \frac{\sum_{i=0}^{6} a_i z^{-i}}{\sum_{i=0}^{6} b_i z^{-i}}$$

In figure 2, this transfer function is shown, while in Appendix A the complete descriptions of $H(s)$ and $H(z)$ are given with the values for a_i and b_i.

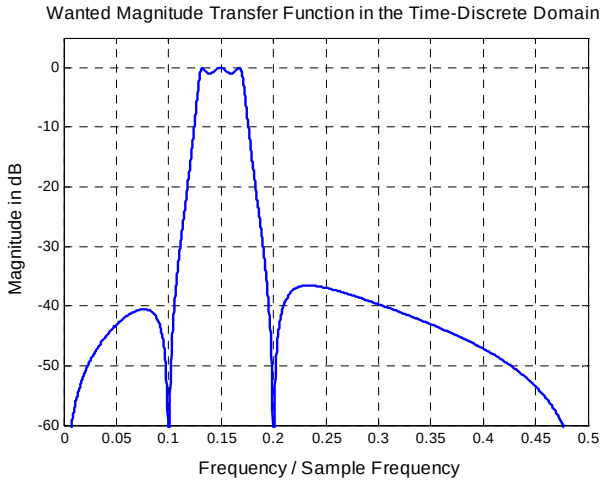


Figure 2. Plot of $H(z)$ to check whether the design specifications are met.

Now there are numerous ways to realize this $H(z)$, but we will restrict ourselves to two implementations based on the Wave Digital Filter theory [3].

Note that neither of the wave digital realizations really need the description of $H(z)$, since they are themselves translations from $H(s)$.

IV. Wave Digital Ladder Realization

For the time-continuous $H(s)$ we are able to find the lossless ladder realization shown in figure 3.

Although the element values are highly unrealistic for an implementation with practical lumped elements, this is no limitation for using it as the prototype for a Wave Digital Filter (WDF).

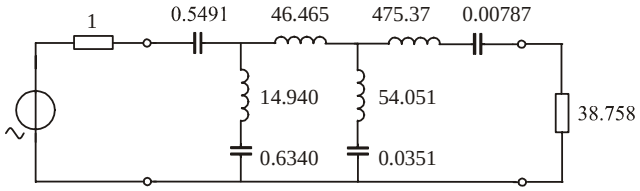


Figure 3. Lossless ladder realization of the 6th order bandpass transfer function.

Transforming this ladder into a wave digital ladder realization by Fettweis's methods is straightforward and the figure 4 adapter structure can be obtained. This wave digital realization has only 9 multiplier coefficients, with values always between −2 and +2: three-port adapters 1 to 7 needing one multiplier each, with adapter 8 needing two of them. This compares favorably with the number of coefficients that would be needed if the transfer function had been realized with p.e. an IIR structure using three 2nd order sections.

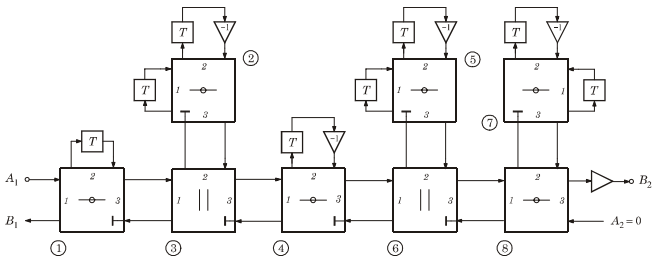


Figure 4. Wave Digital Filter translation of the lossless ladder shown in Figure 3.

Inherent to this implementation method, however, is the fact that for an optimal use of the input and output wordsizes for sinusoidal signals, internal wordsizes have to be scaled by several additional bits to avoid clipping or overflows to occur.

We described the WD ladder using System Generator for DSP 3.1 from Xilnx/MATLAB [5]. This program is very useful for simulation, debugging and description of the circuitry to be used, while promising bit true and cycle true translation into hardware. We found this solution not very attractive for fully automated designs, while in its current state it still has some omissions which need the use of top level VHDL files to set things straight, p.e. for connecting clock signals.

V. WAVE DIGITAL LATTICE REALIZATION

Because the continuous time domain filter realization is electrical symmetric (for the scattering matrix we have $S_{11} = S_{22}$), we can find a symmetrical Lattice realization too. A wave digital translation of this Lattice (LWDF) leads to the structure with two parallel all-passes shown in figure 5. The overall transfer function is determined by the difference in phase characteristics in the two parallel arms. Both all-pass functions are realized with 2nd order two-port adapter sections.

The three blocks *H* in figure 5a all have the structure shown in figure 5b. Each adapter shown in these structures has the architecture of figure 5c. It means that this Lattice realization needs only 6 multiplier coefficients, which equals the filter order.

According to Gazsi [4], these coefficients simply follow from the roots of the denominator of *H*(*s*) in a straightforward way, with values between 0 and +1. Although Gazsi's formulas are derived for odd order lowpass and highpass filters only, his theory holds true for our type of bandpass filter.

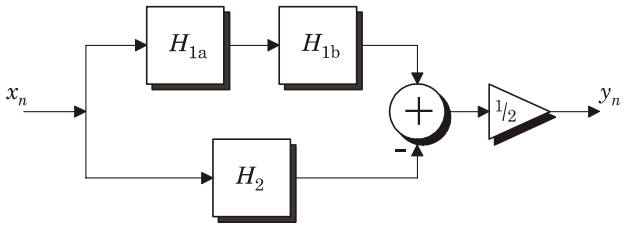
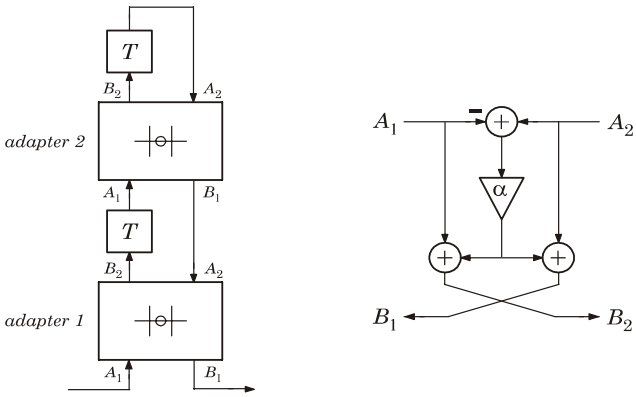


Figure 5a. Structure of the Lattice Wave Digital Filter.



Figures 5b and 5c. Details of the 2nd order adapter sections and each adapter's architecture.

VI. Implementation in Xilinx FPGA: Virtex-II

Because the WD Lattice structure is a highly regular and predictable architecture, automatic generation of complete VHDL descriptions is feasible.

The entire design trajectory (shown in figure 6) has been built to work under MATLAB program control. To design the Lattice version of our example filter, we just enter the command-line

```
lwdf2XDK(6,1,[0.13 0.17],[0.1 0.2])
```

From these filter design parameters we calculate the Lattice coefficients and then build the VHDL description file. This description, together with some pre-written files, is then synthesized (using Synplify Pro from Synplicity) and placed and routed onto the FPGA present on the development kit (using ISE5.2i from Xilinx). Next, the resulting bitfile is downloaded into the FPGA itself. The clock frequency to be used, can again be specified and changed at will from MATLAB.

A. *XtremeDSP Development Kit*

The bitfile is tailored to fit in the User FPGA of an XtremeDSP Development Kit. This board is a development from Nallatech Ltd. that is distributed by Xilinx [6,7]. For our use, it features two ADC channels (14 bits, up to 65 MSPS), two DAC channels (also 14 bits, up to 160 MSPS), a Virtex-II user programmable XC2V3000 FPGA with a.o. 96 embedded 18x18 bits multipliers. To communicate with the board from MATLAB, Nallatech offers the FUSE MATLAB Toolbox [8].

B. *FPGA layout.*

In figure 7 we show a layout picture of the 6th order Lattice bandpass filter mapped onto the Virtex-II chip.

As an option in our program, a designer can choose whether to map a multiplier on a MULT18X18 embedded Virtex multiplier, or to use LUTs for shift and add synthesized multipliers, e.g. to preserve the hardwired ones for other tasks in a complex design. In the layout figure given here, one multiplier which only showed three 1's in its 18 bit binary value was constructed using LUTs. The complete filter was constrained to be located in the lower right corner of the FPGA (which was empty except for the filter) to keep connections to the predefined I/O pins relatively short. Less than 1.5% of the available slices are taken by the filter.

Without any optimization, the filter performed well for sample frequencies up to 30 MSPS.

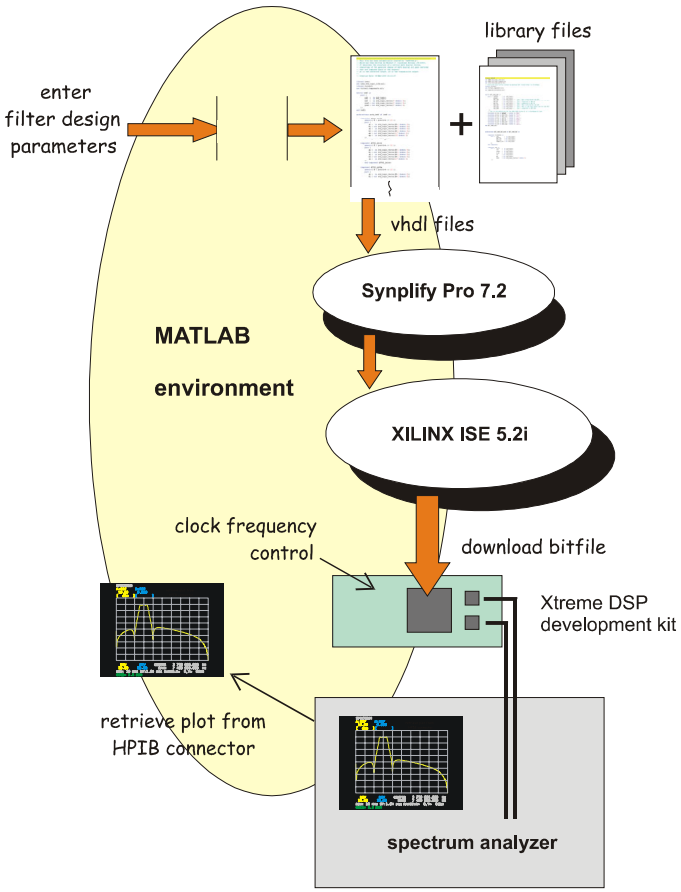


Figure 6. The design trajectory, illustrating that MATLAB is under control from input specification up to plot readback.

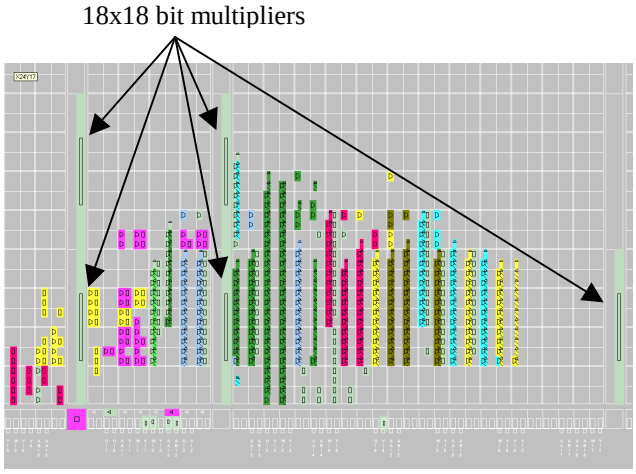


Figure 7. Zoomed-in layout of the LWDF, extracted from the Xilinx floorplanner.

C. *Spectrum analyzer results*

In figure 8 we show a measured frequency characteristic, with the sampling frequency set to 15 MHz.

The passband characteristic frequencies were exactly at their calculated positions, while the two stopband zeros were found to deviate less than 0.1% from the specified values. Due to Sample&Hold distortion a slight roll-off of 0.01 dB could be seen between the left– and the rightmost peak in the passband.

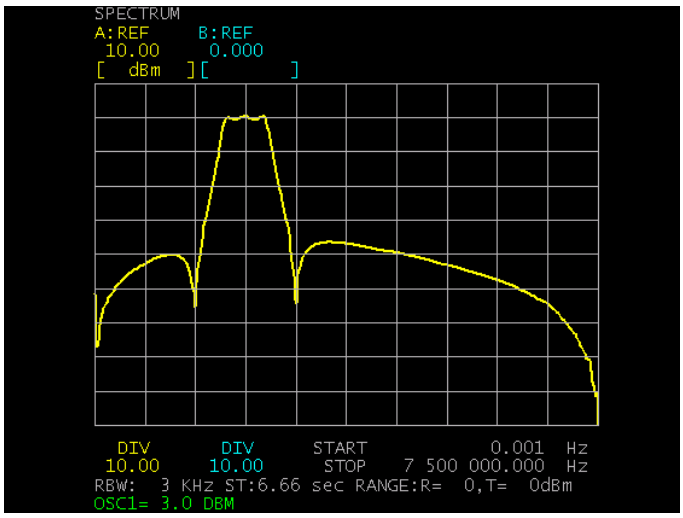


Figure 8. Spectrum analyzer result showing the fundamental interval of the LWDF's magnitude transfer function for a sampling frequency of 15 MSPS.

VII. Conclusions

It has been shown, that we are able to design bandpass filters with a Chebyshev equiripple approximation of the passband and transmission zeros at arbitrary frequencies in the stopbands, and that these designs can be realized as Wave Digital Filters. Gazsi [4] has shown that the Lattice coefficients can be calculated easily. Also, the Lattice structure is notably simpler compared to the wave digital ladder. The coefficients in the Lattice need more accuracy because the Lattice has worse sensitivity properties in the stopband compared to the ladder. The Lattice can be pipelined very easily, making a very high sampling frequency possible. FPGA's turn out to be an ideal platform for implementation of Wave Digital Filters.

The design trajectory that has been illustrated is part of a MATLAB system of programs meant to make wave digital filters more easily designed and used. This system will be made available on an internet site soon.

References

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[5] Xilinx System Generator for DSP version 3.1, Xilinx Inc.

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[7] Virtex-II Platform FPGA Handbook (UG002), Xilinx,Inc.

[8] FUSE MATLAB Toolbox Developers Guide, Nallatech Ltd.

A. Appendix

The transfer functions $H(s)$ and $H(z)$ that have been found for the example filter are:

$$H(s) = \frac{s^5 + 0.63344s^3 + 0.055728s}{74.731s^6 + 11.577s^5 + 59.971s^4 + 6.2195s^3 + 15.421s^2 + 0.76966s + 1.2693}$$

$$H(z) = \frac{\left(0.99439 - 2.2235z^{-1} + 1.9888z^{-2} - 1.9888z^{-4} + 2.2235z^{-5} - 0.99439z^{-6}\right)\cdot 10^{-2}}{1.0000 - 3.3738z^{-1} + 6.5225z^{-2} - 7.6002z^{-3} + 6.0121z^{-4} - 2.8648z^{-5} + 0.78246z^{-6}}$$