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# **Scheduling Toolbox for MATLAB**

## **Reference Guide**

**Version 1.0**

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Scheduling Toolbox for MATLAB *Reference Guide*  
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## Categorical Listing of Functions

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MATLAB resource descriptions simulating their VHDL behavior	
ALU	Simulate the behavior of the VHDL description of a registered ALU.
MUL	Simulate the behavior of the VHDL description of a Multiplier.

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Scheduling functions	
ALAP	Find the SSG using the ALAP method.
ASAP	Find the SSG using the ASAP method.
forceD	Find the SSG using the Force Directed Scheduling method.
listSched	Find the SSG using a List Scheduling method.

---

Fixed-point translation and manipulation functions	
fi xp2hex	Convert a signed value to a hex string represented by fxd-bits.
hex2fi xp	Convert a hex string given by fxd-bits into its signed decimal equivalent.
toSFi xp	Converts a signed fractional value to fit in SFxd bits.
toUFi xp	Converts a signed fractional value to fit in UFxd bits.

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Info, Graph and schedule viewers	
ci rI nfo	Extract and display some information from a .cir-file.
read_OUT	Convert the hex data in an .OUT-file into decimal format.
schedGUI	M-file for schedGUI.fig
showDi stri b	Plot resource usage versus clock STATES.
showGraph	Converts 'graph.dot' to an image and opens a viewer to show it.
vi ew_ci r_I O	Graphical view of input circuit description.
xpl ore	Plot design evaluation space information for a cir-file description.

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Testbench and MATLAB / VHDL file generators	
gen_mTB	Create MATLAB reference testbench files.
gen_VHD	Create testbench, wrapper and SSG-module VHDL-files.

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Utilities, mostly for internal use only	
axDrag2	Pan and zoom with mouse and simple keystrokes.
groupI Os	For internal use only.
hpgPl ot	Plot a .hpg-file in schedGUI's preview window.
l i feTi mes	For internal use only (registered outputs in resources assumed).
mapResources	For internal use only (registered outputs in resources assumed).
parse	Read and convert a .cir-file into internal data format.
schedul e	Determines a time schedule (SSG).
showREGs	Plot REGister usage.
start up	Setup paths for msclab_et4054.
toAdj Mat	Converts an interconnection table into an adjacency matrix.

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#### Graphical User Interface

schedGUI	GUI that combines most of the above mentioned functions.
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## Alphabetical Listing of Functions

### *for general use*

ALAP	Find the SSG using the ALAP method.
ALU	Simulate the behavior of the VHDL description of a registered ALU.
ASAP	Find the SSG using the ASAP method.
ci r I nfo	Extract and display some information from a .cir-file.
fi xp2hex	Convert a signed value to a hex string represented by fxd-bits.
forceD	Find the SSG using the Force Directed Scheduling method.
gen_I NP	Write data into the correct format for an .INP-file.
gen_mTB	Create MATLAB reference testbench files.
gen_VHD	Create testbench, wrapper and SSG-module VHDL-files.
hex2fi xp	Convert a hex string given by fxd-bits into its signed decimal equivalent.
l i stSched	Find the SSG using a List Scheduling method.
MUL	Simulate the behavior of the VHDL description of a MULtiplier.
parse	Read and convert a .cir-file into internal data format.
read_OUT	Convert the hex data in an .OUT-file into decimal format.
schedGUI	M-file for schedGUI.fig
showDi stri b	Plot resource usage versus clock STATES.
showGraph	Converts 'graph.dot' to an image and opens a viewer to show it.
toAdj Mat	Converts an interconnection table into an adjacency matrix.
toSFi xp	Converts a signed fractional value to fit in SFxd bits.
toUFi xp	Converts a signed fractional value to fit in UFxd bits.
vi ew_ci r_I O	Graphical view of input circuit description.
xpl ore	Plot design evaluation space information for a cir-file description.

### *for internal use only*

axDrag2	Pan and zoom with mouse and simple keystrokes.
groupI Os	For internal use only.
hpgPI ot	Plot a .hpg-file in schedGUI's preview window.
l i feTi mes	For internal use only (registered outputs in resources assumed).
mapResources	For internal use only (registered outputs in resources assumed).
schedul e	Determines a time schedule (SSG).
showREGs	Plot REGister usage.
startup	Setup paths for msclab_et4054.

# ALAP

**Purpose** Find the SSG using the ALAP method.

**Syntax** `tFrames = ALAP(adj Mat, delayVec)`

**Description** `tFrames = ALAP(adj Mat, delayVec)` returns a two-column vector `tFrames` describing the SSG (Scheduled Sequencing Graph) of the operations when scheduled according to the ALAP (As Late As Possible) method (no resource constraints).  
The unscheduled flow has to be given in `adj Mat` with the clock delays per resource type (e.g. MUL, ALU) as integer number of clock cycles specified in `delayVec`.

## Examples

**See Also**

<code>ASAP</code>	Find the SSG using the ASAP method.
<code>forceD</code>	Find the SSG using the Force Directed Scheduling method.
<code>ListSched</code>	Find the SSG using the List Scheduling method.
<code>parse</code>	Read and convert a .cir-file into internal data format.
<code>toAdj Mat</code>	Converts an interconnection table into an adjacency matrix.

# ALU

**Purpose** Simulate the behavior of the VHDL description of a registered ALU.

**Syntax** `result = ALU(op1, op2, fxd, opcode)`

**Description** `result = ALU(op1, op2, fxd, opcode)` returns the result of the operation as specified in `opcode`. Here `op1` and `op2` are two signed fixed-point input variables, while `result` is the output in the same signed fixed-point format. This format has to be given in the vector `fxd` as `[N M]`, where `N` denotes the total number of bits, while `M` defines the number of fractional bits. Valid opcodes are 'add' and 'sub'.

`[result, overflow] = ALU(op1, op2, fxd, opcode, ovMode)` also signals the correctness of the result in 'overflow'. A zero means that the result is unaltered and correct, `overflow = 1` means that the result has been 'wrapped' (e.g. bits left of msb has been skipped) if `ovMode = 'wrap'` (the default choice), or has been saturated to its highest positive value or lowest negative value when `ovMode = 'sat'` has been specified.

## Examples

**See Also** `MUL` simulate the behavior of the VHDL description of a registered multiplier.



# ASAP

**Purpose** Find the SSG using the ASAP method.

**Syntax** `tFrames = ASAP(adj Mat, delayVec)`

**Description** `tFrames = ASAP(adj Mat, delayVec)` returns a two-column vector `tFrames` describing the SSG (Scheduled Sequencing Graph) of the operations when scheduled according to the ASAP (As Soon As Possible) method (no resource constraints).  
The unscheduled flow has to be given in `adj Mat` with the clock delays per resource type (e.g. MUL, ALU) as integer number of clock cycles specified in `delayVec`.

## Examples

**See Also**

<code>ALAP</code>	Find the SSG using the ALAP method.
<code>forceD</code>	Find the SSG using the Force Directed Scheduling method.
<code>ListSched</code>	Find the SSG using the List Scheduling method.
<code>parse</code>	Read and convert a .cir-file into internal data format.
<code>toAdj Mat</code>	Converts an interconnection table into an adjacency matrix.

## **cirInfo**

---

**Purpose** Extract and display some information from a .cir-file.

**Syntax** `ci rI nfo(ci rFi l ename)`

**Description** `ci rI nfo` lists in the console window the total number of operations, and the numbers of multiplications, ALU operations, coefficients, and delay elements. Also the number of external inputs and outputs are listed, followed by the input and output identifier names.  
`ci rI nfo` can be used as a first test to check a .cir-file for the absence of errors.

**Examples**

```
>> cirInfo('FIR5.cir')
totally 11 operations, of which
      6 multiplications, and
      5 ALU operations.
  6 constant coefficients
  5 delay elements
  1 input(s) : i0
  1 output(s): o5
>>
```

**See Also**

## fixp2hex

<b>Purpose</b>	Convert a signed value to a hex string represented by <code>fxd</code> -bits.						
<b>Syntax</b>	<code>hexStr = fi xp2hex(decVal , fxd)</code>						
<b>Description</b>	<p><code>hexStr = fi xp2hex(decVal , fxd)</code> checks whether the decimal figure <code>decVal</code> fits in the given <code>fxd</code> bits and if so, returns its hexadecimal representation as a string.</p> <p><code>fxd</code> is supposed to be a two-element vector <code>[N M]</code>, where <code>N</code> defines the total number of available bits and <code>M</code> defines the number of bits to the right of the binary point.</p> <p>If <code>M</code> is too low to exactly represent <code>decVal</code>, <code>decVal</code> will be truncated.</p> <p>An error message is issued when <code>N-M</code> should be too low to represent the signed integer part of <code>decVal</code>.</p> <p><code>decVal</code> itself can be a vector of fractional decimals.</p>						
<b>Examples</b>							
<b>See Also</b>	<table><tr><td><code>hex2fi xp</code></td><td>Convert a hex string given by <code>fxd</code>-bits into its signed decimal equivalent.</td></tr><tr><td><code>toSfi xp</code></td><td>Converts a signed fractional value to fit in <code>SFxd</code> bits.</td></tr><tr><td><code>toUfi xp</code></td><td>Converts an unsigned fractional value to fit in <code>UFxd</code> bits.</td></tr></table>	<code>hex2fi xp</code>	Convert a hex string given by <code>fxd</code> -bits into its signed decimal equivalent.	<code>toSfi xp</code>	Converts a signed fractional value to fit in <code>SFxd</code> bits.	<code>toUfi xp</code>	Converts an unsigned fractional value to fit in <code>UFxd</code> bits.
<code>hex2fi xp</code>	Convert a hex string given by <code>fxd</code> -bits into its signed decimal equivalent.						
<code>toSfi xp</code>	Converts a signed fractional value to fit in <code>SFxd</code> bits.						
<code>toUfi xp</code>	Converts an unsigned fractional value to fit in <code>UFxd</code> bits.						

## forceD

**Purpose** Find the SSG using the Force Directed Scheduling method.

**Syntax** `tFrames = forceD(adj Mat, mul Ops)`

**Description** `tFrames = forceD(adj Mat, mul Ops)` returns a two-column vector `tFrames` describing the SSG (Scheduled Sequencing Graph) of the operations when scheduled according to the Force Directed Scheduling method with optimal resource distribution.

**NOTE:** At the moment, the latency of the resources (MUL, ALU) is expected to be one clock cycle.

The unscheduled flow has to be given in `adj Mat`, while in the vector `mul Ops` the resource type of the operations should be specified ( a 1 means a multiplication).

### Examples

**See Also**

<code>ALAP</code>	Find the SSG using the ALAP method.
<code>ASAP</code>	Find the SSG using the ASAP method.
<code>ListSched</code>	Find the SSG using the List Scheduling method.
<code>parse</code>	Read and convert a .cir-file into internal data format.
<code>toAdj Mat</code>	Converts an interconnection table into an adjacency matrix.

**Reference** *Force-Directed Scheduling for the Behavioral Synthesis of ASIC's*,  
Pierre G. Paulin and John P. Knight,  
IEEE Trans on Computer-Aided Design, Vol. 8, No. 6, JUNE 1989, pages 661-679

## gen\_INP

**Purpose** Write data into the correct format for an .INP-file.

**Syntax** gen\_INP(inpFileName, fxd, coeffs, inpSig)

**Description** gen\_INP(inpFileName, fxd, coeffs, inpSig) creates the file inpFileName and writes sequentially first all coefficients line by line, and next inpSig line by line in a VHDL hex representation of the fxd format to this file. The format and the start of the coefficients and the input sections will be marked with comment lines. All data values are 'rounded' before they are converted to fixed-point.

### Examples

```
>> load coeffs_FIR5.mat
>> coeffs
coeffs =
    'c0'    [-0.07556556070608]
    'c1'    [ 0.09129209297815]
    'c2'    [ 0.47697917208036]
    'c3'    [ 0.47697917208036]
    'c4'    [ 0.09129209297815]
    'c5'    [-0.07556556070608]
>> gen_INP('FIR5.INP', [17 15], coeffs, -1:0.4:1 )
>> type FIR5.INP

-- [17 15] fixed-point format
-- coefficients: c0,c1,c2,c3,c4,c5
x"1F654"
x"00BAF"
x"03D0E"
x"03D0E"
x"00BAF"
x"1F654"
-- input function
x"18000"
x"1B333"
x"1E666"
x"0199A"
x"04CCD"
x"08000"
>>
```

**.INP-file format** See Chapter “INP and OUT-files”.

**See Also** read\_OUT Convert the hex data in an .OUT-file into decimal format.

## gen\_mTB

<b>Purpose</b>	Create MATLAB reference testbench files.
<b>Syntax</b>	<pre>gen_mTB(cirFilename, toScreen, schedMethod, varargin) coeffsSeq = GEN_MTB(cirFilename, toScreen, schedMethod, varargin)</pre>
<b>Description</b>	<p>gen_mTB(cirFilename, toScreen, schedMethod, varargin) creates two MATLAB files: a description of the SSG given in cirFilename, and a testbench-file which calls this SSG.</p> <p>If toScreen is 1, these are written to the screen; if 0, they are written to disk. If cirFilename should be NAME.cir, they can be found in (a newly created directory) NAME\matlab.</p> <ul style="list-style-type: none"><li>The (top-level) testbench-file will be named testbench_NAME_auto.m (see its HELP function), the SSG-file TB_NAME_auto.m. Input data for the testbench is expected to be found (line by line) in a (user created) file named NAME.INP, and output will be written to a file NAME.OUT, both in the directory NAME\matlab.</li></ul> <p>schedMethod specifies the scheduling method to be used, and can be 'ASAP', 'ALAP', 'forced' or 'LIST'.</p> <p>The parameters that follow schedMethod (indicated with varargin here) are dependant on the method chosen, and may be values for delayMUL, delayALU, nMULs and/or nALUs:</p> <ul style="list-style-type: none"><li>delayMUL and delayALU are the latencies of resp. MULTIpliers and ALUs in integer multiples of a clock cycle. They are optional for 'ASAP' and 'ALAP' (default, if not specified, is 1 cycle each). At this moment they are not needed for 'forced' (both fixed to 1). For the 'LIST' method, each of the delays needs to be specified.</li><li>nMULs and nALUs are the number of available MULTIpliers and ALUs, and have to be specified for the 'LIST' method only.</li></ul> <p>coeffsSeq = gen_mTB(cirFilename, toScreen, schedMethod, varargin) also returns the names and the order of the coefficients that are expected in the .INP-file.</p> <p><b>NOTE 1:</b> gen_mTB expects to be run from the directory in which the .cir-file resides.</p> <p><b>NOTE 2:</b> The fixed-point format of the .INP-file should always match the format that is passed to the testbench.</p>
<b>Examples</b>	<pre>gen_mTB('my_file.cir', 1, 'asap' ) gen_mTB('my_file.cir', 0, 'al ap', 2, 1 ) gen_mTB('my_file.cir', 0, 'forced' ) coeffsSeq = gen_mTB('my_file.cir', 0, 'list', 1, 1, 3, 2 )  &gt;&gt; help testbench_my_file_auto Syntax: TESTBENCH_my_file_AUTO(SFxd3,DBG)</pre>

---

SFxd3 defines width of signed fractional fixed-point databus in vector [N M x], where N is the total number of bits of the external I/O bus from which M are fractional bits.  
x defines an additional number of bits with which N should be extended inside the SSG.  
If DBG = 1, intermediate results are printed.  
Needs 'MY\_FILE.INP' in current directory to read input data from, writes 'MY\_FILE.OUT' with results.

**.INP-file format** See Chapter “**INP and OUT-files**”.

**See Also** gen\_VHD Create testbench, wrapper and SSG VHDL-files.

## gen\_VHD

<b>Purpose</b>	Create testbench, wrapper and SSG-module VHDL-files.
<b>Syntax</b>	<code>gen_VHD (ci rFi l ename, SFxd3, toScreen, schedMethod, varargi n)</code>
<b>Description</b>	<p><code>gen_VHD(ci rFi l ename, SFxd3, toScreen, schedMethod, varargi n)</code> creates the VHDL files needed for simulation and synthesis ( a testbench, a wrapper and the SSG-module VHDL-files).</p> <p><code>SFxd3</code> should be a 3-element vector <code>[N M x]</code>, in which <code>N</code> indicates the external buswidth (signed fixed-point), <code>M</code> the number of bits of <code>N</code> to be used for the fraction part, and <code>x</code> an additional number of bits for extending (the whole-number part of) <code>N</code> inside the SSG (to allow for intermediate results greater or less than can be represented with <code>N</code> bits).</p> <p>If <code>toScreen</code> is 1, the files are written to the screen; if 0, they are written to disk. If <code>ci rFi l ename</code> should be <code>NAME. ci r</code>, they can be found in (a newly created directory) <code>NAME\vhdl</code> .</p> <p>The (top-level) testbench-file will be named <code>testbench_NAME_auto. vhd</code>, the wrapper file <code>NAME_auto. vhd</code>, and the SSG-file <code>NAME_SSG_auto. vhd</code>. For simulation all <code>vhd</code>-files placed in the directory are needed, e.g. also the files <code>resources_regd. vhd</code> and <code>txt_util2. vhd</code>. Input data for the testbench is expected to be found (line by line) in a (user created) file named <code>NAME. I NP</code>, and output will be written to a file <code>NAME. OUT</code></p> <p>Synthesis needs the files <code>resources_reg. vhd</code>, <code>NAME_SSG_auto. vhd</code> and as top level file <code>NAME_auto. vhd</code>.</p> <p><code>schedMethod</code> specifies the scheduling method to be used, and can be 'ASAP' , 'ALAP' , 'forced' or 'LI ST' .</p> <p>The parameters that follow <code>schedMethod</code> (indicated with <code>varargi n</code> here) are dependant on the method chosen, and may be values for <code>del ayMUL</code>, <code>del ayALU</code>, <code>nMULs</code> and/or <code>nALUs</code>:</p> <ul style="list-style-type: none"><li>• <code>del ayMUL</code> and <code>del ayALU</code> are the latencies of resp. MULtipliers and ALUs in integer multiples of a clock cycle. They are optional for 'ASAP' and 'ALAP' (default, if not specified, is 1 cycle each). At this moment they are not needed for 'forced' (both fixed to 1). For the 'LI ST' method, each of the delays needs to be specified.</li><li>• <code>nMULs</code> and <code>nALUs</code> are the number of available MULtipliers and ALUs, and have to be specified for the 'LI ST' method only.</li></ul> <p><b>NOTE 1:</b> <code>gen_VHD</code> expects to be run from the directory in which the <code>.ci r</code>-file resides.</p> <p><b>NOTE 2:</b> The fixed-point format of the <code>.I NP</code>-file should always match the format that is passed to the testbench.</p>
<b>Examples</b>	<pre>gen_VHD( 'my_fi l e. ci r' , [16 15 0], 1, 'asap' ) gen_VHD( 'my_fi l e. ci r' , [16 15 2], 0, 'al ap' , 2, 1 ) gen_VHD( 'my_fi l e. ci r' , [32 30 4], 0, 'forced' ) gen_VHD( 'my_fi l e. ci r' , [24 20 8], 0, 'l i s t' , 1, 1, 3, 2 )</pre>



---

The command

```
>> gen_VHD( 'FIR5.ci r', [17 15 1], 0, 'asap' )
```

will result in an entity definition in FIR5\_auto.vhd that looks like:

```
entity FIR5 is
  generic ( N_g      : positive := 17;
            M_g      : positive := 15;
            NX_g     : positive := 18;
            MUL_delay_g : Time := 5 ns;
            ALU_delay_g : Time := 2 ns;
            REG_delay_g : Time := 2 ns );
  port ( Clk      : in std_logic;
        Reset    : in std_logic;
        New_Sample : in std_logic;
        C0 : in std_logic_vector(N_g-1 downto 0);
        C1 : in std_logic_vector(N_g-1 downto 0);
        C2 : in std_logic_vector(N_g-1 downto 0);
        C3 : in std_logic_vector(N_g-1 downto 0);
        C4 : in std_logic_vector(N_g-1 downto 0);
        C5 : in std_logic_vector(N_g-1 downto 0);
        I0 : in std_logic_vector(N_g-1 downto 0);
        O5 : out std_logic_vector(N_g-1 downto 0);
        Done      : out std_logic;
        Error     : out std_logic
  );
end FIR5;
```

**See Also**      gen\_mTB      Create MATLAB reference testbench files.

## hex2fixp

<b>Purpose</b>	Convert a hex string given by <code>fxd</code> -bits into its signed decimal equivalent.						
<b>Syntax</b>	<code>decVal = hex2fixp(hexStr, fxd)</code>						
<b>Description</b>	<p><code>decVal = hex2fixp(hexStr, fxd)</code> converts <code>hexStr</code> into a (possibly fractional) signed decimal value in <code>fxd</code> bits.</p> <p><code>fxd</code> is supposed to be a two-element vector <code>[N M]</code>, where <code>N</code> defines the total number of available bits and <code>M</code> defines the number of bits to the right of the binary point.</p> <p>An error message is issued when <code>decVal</code> cannot be represented in the given <code>fxd</code> bits.</p> <p><code>hexStr</code> can be an array of strings.</p> <p><b>NOTE:</b> usually MATLAB's 'format long' will be necessary to represent the result with enough decimals (avoid rounding to 'short' format).</p>						
<b>Examples</b>							
<b>See Also</b>	<table><tr><td><code>fixp2hex</code></td><td>Convert a signed value to a hex string represented by <code>fxd</code>-bits.</td></tr><tr><td><code>toSFfixp</code></td><td>Converts a signed fractional value to fit in <code>SFxd</code> bits.</td></tr><tr><td><code>toUFixp</code></td><td>Converts an unsigned fractional value to fit in <code>UFxd</code> bits.</td></tr></table>	<code>fixp2hex</code>	Convert a signed value to a hex string represented by <code>fxd</code> -bits.	<code>toSFfixp</code>	Converts a signed fractional value to fit in <code>SFxd</code> bits.	<code>toUFixp</code>	Converts an unsigned fractional value to fit in <code>UFxd</code> bits.
<code>fixp2hex</code>	Convert a signed value to a hex string represented by <code>fxd</code> -bits.						
<code>toSFfixp</code>	Converts a signed fractional value to fit in <code>SFxd</code> bits.						
<code>toUFixp</code>	Converts an unsigned fractional value to fit in <code>UFxd</code> bits.						

## listSched

<b>Purpose</b>	Find the SSG using a List Scheduling method.										
<b>Syntax</b>	<code>tFrames = listSched(adj Mat, delayVec, mul Ops, nMULs, nALUs)</code>										
<b>Description</b>	<code>tFrames = listSched(adj Mat, delayVec, mul Ops, nMULs, nALUs)</code> returns a two-column vector 'tFrames' describing the SSG (Scheduled Sequencing Graph) of the operations when scheduled according to a specified List Scheduling method under resource constraints. The unscheduled flow has to be given in <code>adj Mat</code> with the latency per resource type (e.g. MUL, ALU) as integer number of clock cycles specified in <code>delayVec</code> . In the vector <code>mul Ops</code> the resource type of the operations should be given (a 1 means a multiplication), and the available numbers of resources in <code>nMULs</code> and <code>nALUs</code> .										
<b>Examples</b>											
<b>See Also</b>	<table><tr><td>ALAP</td><td>Find the SSG using the ALAP method.</td></tr><tr><td>ASAP</td><td>Find the SSG using the ASAP method.</td></tr><tr><td>listSched</td><td>Find the SSG using the List Scheduling method.</td></tr><tr><td>parse</td><td>Read and convert a .cir-file into internal data format.</td></tr><tr><td>toAdj Mat</td><td>Converts an interconnection table into an adjacency matrix.</td></tr></table>	ALAP	Find the SSG using the ALAP method.	ASAP	Find the SSG using the ASAP method.	listSched	Find the SSG using the List Scheduling method.	parse	Read and convert a .cir-file into internal data format.	toAdj Mat	Converts an interconnection table into an adjacency matrix.
ALAP	Find the SSG using the ALAP method.										
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parse	Read and convert a .cir-file into internal data format.										
toAdj Mat	Converts an interconnection table into an adjacency matrix.										

# MUL

<b>Purpose</b>	Simulate the behavior of the VHDL description of a registered MULtiplier.
<b>Syntax</b>	<code>result = MUL(op1, op2, fxd)</code>
<b>Description</b>	<code>result = MUL(op1, op2, fxd)</code> returns the (signed) result of the multiplication of <code>op1</code> and <code>op2</code> (both signed). The binary fixed-point format of <code>result</code> , as well as that of <code>op1</code> and <code>op2</code> should be given in the vector <code>fxd</code> as <code>[N M]</code> , where <code>N</code> denotes the total number of bits, while <code>M</code> defines the number of fractional bits.
<b>Examples</b>	
<b>See Also</b>	<code>ALU</code> simulate the behavior of the VHDL description of a registered ALU.

## parse

**Purpose** Read and convert a .cir-file into internal data format.

**Syntax** `CIRC_Data = parse(i nFile name)`

**Description** `CIRC_Data = parse(i nFile name)` extracts data from a textual circuit description in a .cir-file. The data returned in the structure `CIRC_Data` contains the following fields.

`CIRC_Data.iocDef`  
`CIRC_Data.iConnTbl`  
`CIRC_Data.xConnTbl`  
`CIRC_Data.opTypes`  
`CIRC_Data.opNames`  
`CIRC_Data.inpNames`  
`CIRC_Data.outNames`  
`CIRC_Data.dlyInps`

`CIRC_Data.iocDef` is a string defining the characters that are used as the first character in an `opName` to identify inputs, outputs and constant coefficients with. `CIRC_Data.iConnTbl` is a (number of operations x 4) array that describes the interconnections between the operations. The first column list the operation identification numbers (`opi d#`), where the corresponding type and name of an `opi d#` can be found in `CIRC_Data.opTypes` and `CIRC_Data.opNames` respectively. Columns 2 and 3 list the `opi d#`s of the operations that are connected to this `opi d#`'s inputs. A negative sign is used to indicate that the input is connected to an input port (`inp#`), the name of which can be found as entry `inp#` in the cell-vector `CIRC_Data.inpNames`.

Output ports (`outp#`) are given in column 4, while their names are listed in `CIRC_Data.outNames`.

If no shift operations (`<<` or `>>`) are present, `iConnTbl` is a one dimensional (number\_of\_operations,4) array, else a (number\_of\_operations,4,2) array.

`opTypes`: mul , add, sub, ...

`CIRC_Data.xConnTbl`

`CIRC_Data.dlyInps`

## Examples

**See Also** `GroupI Os` ...

## read\_OUT

**Purpose** Convert the hex data in an .OUT-file into decimal format.

**Syntax**

```
y = READ_OUT(outFilename, fxd2)
y = READ_OUT(outFilename, fxd2, nOutputs)
y = READ_OUT(outFilename, fxd2, nOutputs, nFracDigits)
```

**Description** `y = READ_OUT(outFilename, fxd2)` returns the hex data as read from `outFilename` in a decimal format specified by the vector `fxd2` (`[N M]` fixed-point format). Output is also displayed in the console window.

`y = READ_OUT(outFilename, fxd2, nOutputs)` should be used if the circuit for which `outFilename` is valid, shows more than one outputs. `y` will become a column vector with as many rows as given by `nOutputs`.

`y = READ_OUT(outFilename, fxd2, nOutputs, nFracDigits)` can be used to limit the number of fractional digits that are displayed in the console window (default the sum of the numbers of digits for the whole part, the fractional point and for the fractional part together is 17).

### Examples

```
>> o5 = read_OUT('FIR5\vhdl\FIR5.OUT',[17 15],1,5);
1: x"00000" = 0.00000
2: x"00000" = 0.00000
3: x"00000" = 0.00000
4: x"1F654" = -0.07556
5: x"00203" = 0.01572
6: x"03F11" = 0.49271
7: x"07C1F" = 0.96970
8: x"087CE" = 1.06097
9: x"07E22" = 0.98541
10: x"07E22" = 0.98541
11: x"07E22" = 0.98541
12: x"07E22" = 0.98541
13: x"07E22" = 0.98541
```

**.INP-file format** See Chapter “**INP and OUT-files**”.

**See Also** `gen_INP` Write data into the correct format for an .INP-file.

# showDistrib

**Purpose** Plot resource usage versus clock STATES.

**Syntax** `showDistrib(cirFileName, schedMethod, varargin)`

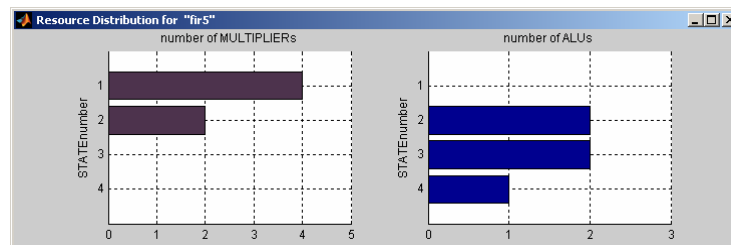
**Description** `showDistrib(cirFileName, schedMethod, varargin)` determines and plot the usage of the MULTIpliers and ALUs for the circuit described in `cirFileName`, when scheduled with the method defined with `schedMethod` and the optionally additional parameters in `varargin`.

`schedMethod` specifies the scheduling method to be used, and can be 'ASAP', 'ALAP', 'forced' or 'LIST'.

The parameters in `varargin` are dependant on the method chosen, and may be values for `delayMUL`, `delayALU`, `nMULs` and/or `nALUs`:

- `delayMUL` and `delayALU` are the latencies of resp. MULTIpliers and ALUs in integer multiples of a clock cycle. They are optional for 'ASAP' and 'ALAP' (default, if not specified, is 1 cycle each). At this moment they are not needed for 'forced' (both fixed to 1). For the 'LIST' method, each of the delays needs to be specified.
- `nMULs` and `nALUs` are the number of available MULTIpliers and ALUs, and have to be specified for the 'LIST' method only.

**Examples** `>> showDistrib('fir5.cir','forced')`



**See Also**

## showGraph

<b>Purpose</b>	Converts 'graph.dot' to an image and opens a viewer to show it.
<b>Syntax</b>	showGraph(gFormat)
<b>Description</b>	SHOWGRAPH(gFormat) displays the image- file that is described in ' graph. dot' , using the intermediate file ' graph. xxx' where xxx is replaced by the string given in gFormat. Valid formats are ' png' , ' j pg' and ' hpg' . Usually, ' graph. dot' will have been created by schedGUI or by schedul e. m.
<b>Examples</b>	
<b>See Also</b>	vi ew_ci r_I0 Graphical view of cir-file description with In- and Outputs shown.



## toAdjMat

<b>Purpose</b>	Converts an interconnection table into an adjacency matrix.
<b>Syntax</b>	<code>adj Mat = TOADJMAT(i connTbl )</code>
<b>Description</b>	<code>adj Mat = TOADJMAT(i connTbl )</code> , where <code>i connTbl</code> usually will be the <code>CIRC_Data.i connTbl</code> output from <code>parse.m</code> . The <code>adj Mat</code> is a.o. needed as input for the scheduling routines such as ASAP, ALAP, etc.
<b>Examples</b>	
<b>See Also</b>	<code>parse</code> Read and convert a .cir-file into internal data format.

## toSFixp

**Purpose** Converts a signed fractional value to fit in SFxd bits.

**Syntax** SFi xVal ue = toSFi xp(decVal , SFxd)

**Description** SFi xVal ue = toSFi xp(decVal , SFxd) truncates (= towards minus infinity), if needed, the signed decimal fractional decVal to fit in the given SFxd bits and returns it in SFi xVal ue.  
SFxd is supposed to be a two-element vector [N M], where N defines the total number of available bits and M defines the number of bits to the right of the binary point. decVal can be a vector of signed fractional decimals.  
SFi xVal ue = toSFi xp(decVal , SFxd, 'round' ) can be used to do a rounding operation instead of just a truncation.

### Examples

**See Also**

fi xp2hex	Convert a signed value to a hex string represented by fxd-bits.
hex2fi xp	Convert a hex string given by fxd-bits into its signed decimal equivalent.
toUFi xp	Converts an unsigned fractional value to fit in UFXd bits.

## toUFixp

**Purpose** Converts an unsigned fractional value to fit in UFixd bits.

**Syntax** UFixValue = toUFixp(decVal, UFixd)

**Description** UFixValue = toUFixp(decVal, UFixd) truncates (= towards minus infinity), if needed, the unsigned decimal fractional decVal to fit in the given UFixd bits and returns it in UFixValue.  
UFixd is supposed to be a two-element vector [N M], where N defines the total number of available bits and M defines the number of bits to the right of the binary point. decVal can be a vector of signed fractional decimals.

### Examples

**See Also**

fixp2hex	Convert a signed value to a hex string represented by fxd-bits.
hex2fixp	Convert a hex string given by fxd-bits into its signed decimal equivalent.
toSFixp	Converts a signed fractional value to fit in UFixd bits.

## view\_cir\_IO

**Purpose** Graphical view of cir-file description with In- and Outputs shown.

**Syntax** `view_cir_IO(cirFilename)`

**Description** `view_cir_IO(cirFilename)` shows the Data Flow Graph that is extracted from the circuit-file `cirFilename` in a platform specific viewer.  
An intermediate file `graph_io.png` will be written in the current directory.

`view_cir_IO(cirFilename, outType)`, where `outType` is a string, can be used to specify different formats of the `graph_io`-file.  
Valid formats besides 'png' are: 'hpg', 'jpg', ...  
If `outType` is empty, the 'png' format will be used.

`view_cir_IO(cirFilename, outType, topBottom)` can be used to specify whether the in and output connections may be displayed inside the graph (`topBottom = 0`, the default value), or should be put on separate top and bottom lines outside the graph (`topBottom = 1`).

### Examples

**See Also** `showGraph` Opens a viewer to show image-file 'graph.xxx'.

## xplore

<b>Purpose</b>	Plot design evaluation space information for a cir-file description.
<b>Syntax</b>	<pre>xplore(cirFilename) xplore(cirFilename, costFacs) xplore(cirFilename, costFacs, delayMUL, delayALU)</pre>
<b>Description</b>	<p><code>xplore(cirFilename)</code> estimates the area or cost involved by different implementations of <code>cirFilename</code> based on the numbers of <code>MULT</code>pliers and <code>ALU</code>s available (and consequently the number of <code>REG</code>isters needed). All registers are taken into account, i.e. the registers needed for life-time extension, but also the feedback register (if present) and registers for each input and each output.</p> <p><code>xplore(cirFilename, costFacs)</code> controls the relative areas, that are taken by <code>MULT</code>pliers, <code>ALU</code>s and <code>REG</code>isters with the vector <code>costFacs</code>. This should be a three element vector giving user definable costs factors for <code>[ mulCost aluCost regCost ]</code>, e.g. <code>[ 2 1.2 0.8 ]</code>.</p> <p><code>xplore(cirFilename, costFacs, delayMUL, delayALU)</code> will perform the scheduling computations with the specified <code>delayMUL</code> and <code>delayALU</code> (both given in integer number of clock cycles).</p>
<b>Examples</b>	
<b>See Also</b>	

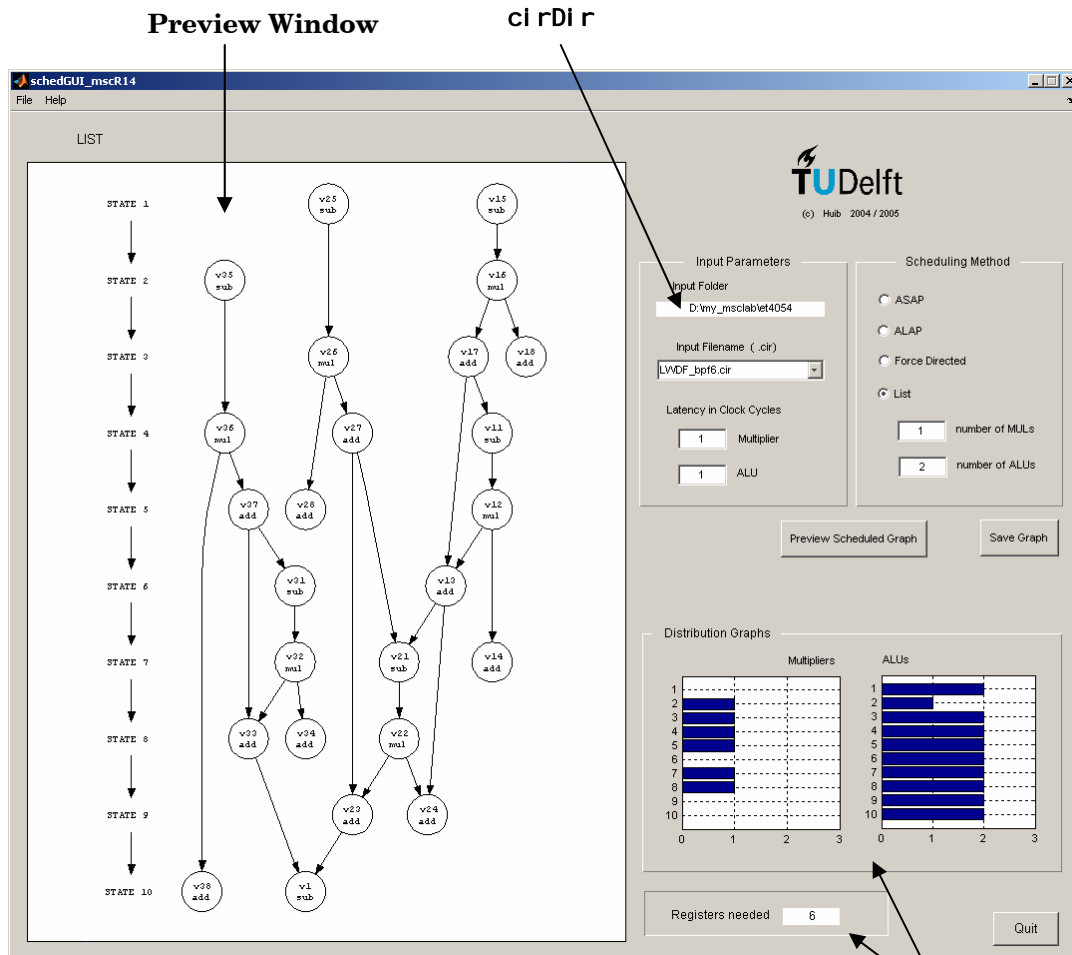
# schedGUI

The Graphical User Interface schedGUI can be used for quickly judging and comparing the results of different scheduling methods and scheduling parameters. It assumes a screen resolution of at least 1280 x 1024 to be displayed completely.

The tool can be started with `schedGUI` or (unfortunately not on MATLAB releases before R14) with `schedGUI ('ci rDi r')`. In case `ci rDi r` is specified, this will be `schedGUI`'s startup directory, otherwise `schedGUI` is started from the current directory. One of the `.cir`-files present in the startup directory can be selected for a scheduling operation.

Available scheduling methods are ASAP, ALAP, Force Directed and a List method. The List method is the only resource constrained method and needs to be informed how many multipliers and ALUs may be used at the same time.

With the ASAP, ALAP and List method, the latencies of the multipliers and ALUs can be specified (in numbers of integer clock cycles). By default, all resources will have a latency of only one clock cycle.



**miscellaneous info**

**Figure 1.** Screen-shot of the SchedGUI.

The result of the scheduling process, the SSG, (executed after pressing the *Preview Scheduled Graph* button) will be made visible in the preview window. It is possible to pan and zoom out or in on this SSG with the mouse or some predefined keys (see the Menu item *Help --> PreviewPane Options*). Together with the SSG, additional information about the distribution of the multipliers and ALUs and the additional number of memory registers is listed.

The resulting SSG can then be written to an image file by pressing the *Save Graph* button. Supported formats in this case are 'png' and 'jpg'.

Switching to another *ci rDi r* is possible by selecting the Menu item *File --> Set Input Folder*.

There is also a Menu item *File --> Print Preview*, but this one is not yet fully functional.

Drawing of the graphs is accomplished with the aid of software provided by the Graphviz (Graph Visualization Software) package. This software has originally been developed by AT&T Research, and is extended with additional tools in the course of time. Nowadays, it is licensed on an open source basis under The Common Public License. See also <http://www.graphviz.org/>

# Structure and syntax of the .cir file

The input for the scheduling software is an ASCII text file (distinguishable by the extension '.cir'), in which basically all assignments (e.g. the operations to be performed) are written line by line. In the cir-file, one has to describe the operations that can be scheduled (a textual representation of a sequencing graph (SG)), and how this SG is connected to the outer world. Here, we will use an additional layer –the ‘feedback and external I/O layer’– around the SG (which after scheduling will be an SSG) in which all feedback operations and connections have to be described: this information is thus a part of the cir-file, although not subjected to the scheduling process.

In fact, the cir-file is a description of a complete circuit (or circuit module).

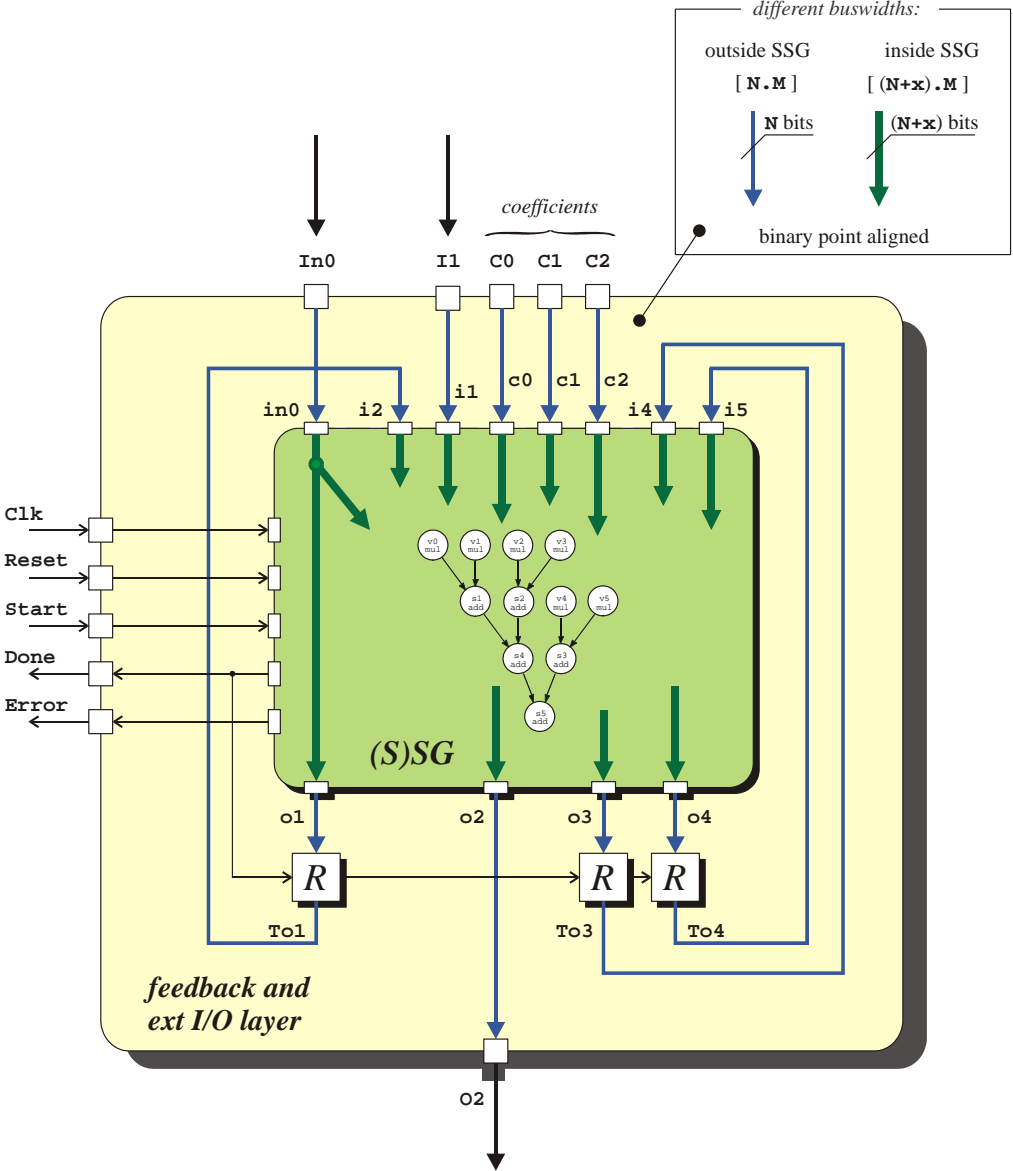


Figure 2. Concept of the cir-file description.



The concept of this setup is shown in Figure 2, for an arbitrary imaginable circuit with 2 external inputs, 1 external output and 3 coefficients.

The operations that are supported in the (S)SG are multiplications (integer shifts, see later), addition and subtractions. The feedback layer is intended for delay elements (registers) and connections. Connections between feedback layer and (S)SG vice versa, and connections to the outside world are established through **Input Ports** and **Output Ports**.

This hierarchy will be maintained when the cir-file is translated into MATLAB m-files and/or when translated into VHDL-entities and architectures.

There are some simple rules that should apply for the .cir-file to be valid:

**Operations** –which perform a multiplication, addition or subtraction– should be identified by a unique 'identifier' name. Such identifiers are also required for all input ports, output ports and coefficient ports. Delays are not part of the (S)SG and are connected to the (S)SG through (internal) input and output ports.

**Identifiers** are case sensitive and may consist only of characters and figures. The first character of an identifier indicates whether the identifier applies to an operation, input port, etc.

By default, identifiers starting with an

    'i' are reserved for input ports,

    'o' are reserved for output ports,

    'a' or 'c' are referring to coefficients (a special kind of inputs),

while all remaining characters can be used to indicate an operation (diacritic characters, underscores, etc. are not allowed).

Each operation will have two (2) inputs and one (1) output:

- **Inputs** are either connected to a previously terminated operation or an input port.
- An input which only appears at the right hand side(s) of (an) assignment(s), and never at a left hand side, is considered to be connected to an external input port.
- The **output** can be either connected to a next-in-line operation or to an output port.
- The result (e.g. the output) of an operation will have the same identifier name as the operation itself.
- Floating input or outputs, as well as floating input ports and output ports, are considered erroneous.

An **Assignment** should have the form

    identifier = identifier operator identifier   with possible operators '\*', '+ and '-'

or

    output port = identifier

or

    input port = Toutput port                    which involves a delayed feedback register

and can be optionally terminated with a ';'.

e.g.

    v1 = v2 + v3;

    i 2 = To1;

Only one assignment per line is allowed.

Note that an input of an operation can be implicitly connected to an input port, as in

    v1 = v2 - i 1;

but that outputs have to be explicitly connected to (only one) operation, e.g.

    o3 = v1;

Also note that it is common sense, given the fact that the names are displayed in output plots, to use relatively short identifiers.

Multiplications that are powers of 2 can be handled more efficiently by using a **'shift'** operation. In hardware, such a shift is just a change in bit-line interconnect.

A shift operation in the cir-file can be specified using the '>>' or '<<' operators.

A shift operation should consist of

- the identifier of the operation, the result of which should be shifted, or an input that should be shifted.
- the shift operator, indicating the direction of the shift: << means a shift to the left (output value is larger than original value), while >> means a shift to the right (decreased output value, power of negative value)
- the integer number of bits (powers of two) to be shifted

this all surrounded by parenthesis.

e.g.

```
v3 = v1 + (v2 >> 2);           % v3 = v1 + v2^(-2)
v1 = (i0 >> 1) - (i0 >> 3);    % v1 = 0.375 * i0;
```

**Note:** The shift operation performs an arithmetic shift to the right, so the sign of the originating value is preserved. For shifts to the left, it's the user's responsibility that the shifted value is handled correctly.

All characters on a line following a '%' are considered to be a comment. The '%' character can be the first one on a line, or can be following an assignment.

If for some reason you are not satisfied with the default start characters, it is possible to define your own identifiers by starting the cir-file (in any case before the first assignment) with the string

```
i ocDef = 'xxxx' ;
```

where

- the first x is replaced with the new character to identify the inputs with,
- the second x with the new character for outputs, and
- the third and fourth x's with new characters for recognizing the coefficients.

e.g.

```
i ocDef = 'XYab' ;
```

Remember that identifiers are case-sensitive.

## Some remarks concerning the VHDL code for simulation and implementation.

Although not mentioned in the cir file, the VHDL code that will be generated for the circuit will define 5 other external control connections, viz.

- input ports for Cl k and Reset,
- ports for the activation and completion signals: Start and Done, as well as
- an additional Error signal that will go high in case of overflow errors during calculations.

The SSG starts calculating at the first positive going clock edge of Cl k, following a low-to-high transition of the Start-signal. At each following positive going Cl k-edge, the next STATE is executed. Finally the Done signal is set high when the output value(s) are valid. Then the process can start all over again (see also the chapter about **Simulation timing setup**).

In the set-up used here, it is expected that the coefficients are passed to the circuit by means of a **.INP**-file. Changing the transfer characteristic of the filter –limited only by the structure used– is then very simple.

It is certainly possible, if the coefficients don't change during a simulation, to have them stored or hardwired in the **feedback and ext I/O layer**. This implies manually editing the VHDL-files or rewriting the MATLAB function.

From a computational point of view, it cannot be assumed that the data busses in the (S)SG should have the same width as in the feedback layer and the outside world. If intermediate computational results in the (S)SG would need additional bits, the bus inside the (S)SG can be made wider than the external bus.

This, however, is not influencing the cir-file and the scheduling process.

It does become crucial when simulating the circuit in MATLAB or VHDL. Indeed, it is with these functions, that this information has to be passed in the form of the fixed-point variables  $[N \ M]$  and  $[N \ M \ x]$ . See the next Chapter, **Signed fixed-point notation**, for a description of this notation.

## Signed fixed-point notation

In most of the Digital Signal Processing designs, calculations are performed with the aid of fixed-point hardware instead of floating-point hardware. The added complexity and hardware resources that are needed by floating-point solutions are always more expensive than fixed-point solutions, and are usually only justifiable for systems with high dynamic ranges. In our filter design, we will also use a fixed-point implementation.

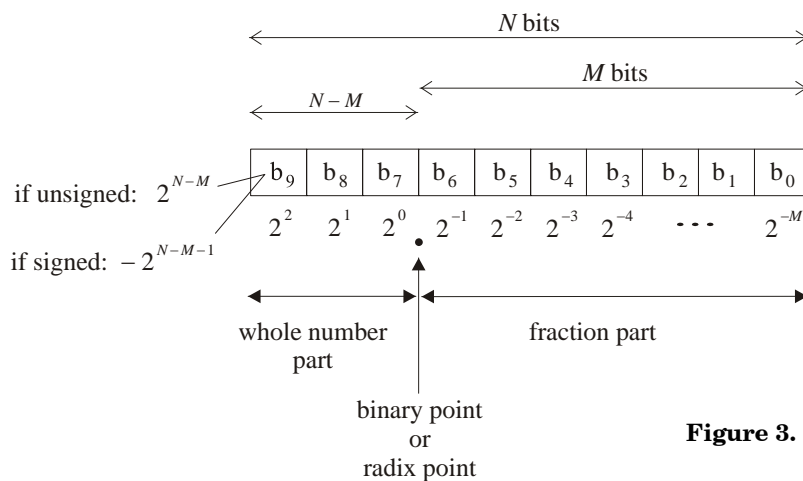
Surely, everyone is acquainted with the all integer representation, i.e. where we are dealing with only positive whole numbers. Since this is a severe limitation in calculations, it is a necessity to also be able to represent negative numbers. For this purpose, the 2's-complement method is the most widely used representation. In this representation, the MSB is assigned a negative weight (see Table B1). The most appealing advantage of this representation is the fact that no additional hardware is needed to perform additions and subtractions; the drawback is that negating a number is not merely an inversion of each bit since the number representation is asymmetrical.

**Table 1.** *N*-bits integer representations (2's complement for signed)

	value	range
unsigned	$N_{UINT} = b_{N-1}2^{N-1} + b_{N-2}2^{N-2} + \dots + b_1s^1 + b_0s^0$	$0 \leq N_{UINT} \leq 2^{N-1}$
signed	$N_{SINT} = -b_{N-1}2^{N-1} + b_{N-2}2^{N-2} + \dots + b_1s^1 + b_0s^0$	$-2^{N-1} \leq N_{SINT} \leq (2^{N-1} - 1)$

However, there is no reason why we should not insert a virtual binary point somewhere between the bits. In fact, for integer representations this point is just assumed to be to the right of the least significant bit. Inserting a binary point influences the weights of each bit, as is indicated in Figure 3, again for an *N* bits fixed point number. We distinguish a 'whole part' and a 'fraction part'.

The binary point itself is generally not coded, but its position has to be known by the software and/or the user: in our notation between the (*M*+1)<sup>th</sup> and the *M*<sup>th</sup> bits from the right.



**Figure 3.** *Fixed-point notation.*

The relation between binary bits and decimal values, and the attainable ranges for these values, are tabulated in Table 2, given an *N* bit binary number of which *M* bits are fraction bits.

**Table 2.**  $[N\ M]$ -bits fixed point representations (2's complement for signed)

	value	range
unsigned	$N_{UMIX} = \sum_{i=M}^{N-1} b_i 2^{i-M} + \sum_{j=0}^{M-1} b_j 2^{j-M}$	$0 \leq N_{UMIX} \leq \left( 2^{N-M} - \frac{1}{2^M} \right)$
signed	$N_{SMIX} = -b_{N-1} 2^{N-M-1} + \sum_{i=M}^{N-2} b_i 2^{i-M} + \sum_{j=0}^{M-1} b_j 2^{j-M}$	$-2^{N-M-1} \leq N_{SMIX} \leq \left( 2^{N-M-1} - \frac{1}{2^M} \right)$

The difference between two consecutive numbers, the resolution, is thus  $\frac{1}{2^M}$ .

A special case is obtained when  $N = M + 1$ . There is only one bit left of the binary point: the weighted sign bit which is either 0 or  $-1$ . All other bits are used to represent a fractional number less than 1. The exact range in this case can be calculated with

$$-1.0 \leq N_{SFRAC} \leq \left( 1 - \frac{1}{2^M} \right)$$

Because of the usually lower number of bits compared with e.g. the number of bits used in MATLAB calculations, the conversion from MATLAB's "doubles" into fixed-point values will most certainly result in quantization errors (worst case errors amounts to  $\left| 2^{-M} \right|$  in case the translation is by truncation, or maximally  $\left| 2^{-M-1} \right|$  in case of rounding).

Together, all these quantization errors determine the final resulting computational accuracy.

In our software we use the notation  $[N\ M]$  to indicate a signed value with totally  $N$  bits, of which  $M$  are used for representing the fraction part: exactly as has been described above.

During the calculations, it is possible that intermediate computational results could only be represented using more than  $N$  bits. This can be the case e.g. when summing a number of positive and negative values, where the resulting value is known to always fit in the  $N$  bits. In such a case, we can increase the number of bits inside the SSG to the left of the MSB with  $x$  bits and denote it as  $[N\ M\ x]$ . Instead of  $N-M$  bits for the whole part, we now use  $N+x-M$  bits for the whole part. The software takes care for an appropriate handling of the sign-bit.

In the ALU. m, MUL. m and resources\_reg. vhd files, one can see how the computations are exactly implemented.

Usually, we will use the hexadecimal (hex) format (also without a visual binary point) instead of the pure binary representation.

## Setup of the .INP- and .OUT-files

The .INP file is an ASCII text file, that can be created with any plain text editor or with the aid of the gen\_INP MATLAB utility.

The .INP file contains

- optionally a number of comment lines (indicated by starting with -- ),
- all coefficients in hexadecimal format,
- optionally a number of comment lines,
- all input data in hexadecimal format.

The sequence in which the values of the coefficients should be entered, has been written in the MATLAB command window when gen\_mTB had been run (normally, this is according to the identifiers of the coefficients sorted in ascending order).

Each data input line represents an input value for an (external) input port. If the circuit contains more than one input, the data lines represent the data for every input port for a particular sample.

If all inputs have been handled, the data for the next sample follows, again for each input port.

An example of a .INP-listing for a 5<sup>th</sup> order FIR-filter (6 coefficients) with an input I0 and an output called O5 is shown below.

### *.INP-file format* ( both for MATLAB and VHDL)

```

-- [17 15] fixed point format
-- coefficients: c0,c1,c2,c3,c4,c5
x"1F654"
x"00BAF"
x"03D0E"
x"03D0E"
x"00BAF"
x"1F654"
-- input function
x"00000"
x"00000"
x"08000"
x"08000"
x"08000"
x"08000"
x"08000"
x"08000"
x"08000"

```

start with the constant coefficients,

followed by the input data sequence to be investigated

hex VHDL format should be used for all data

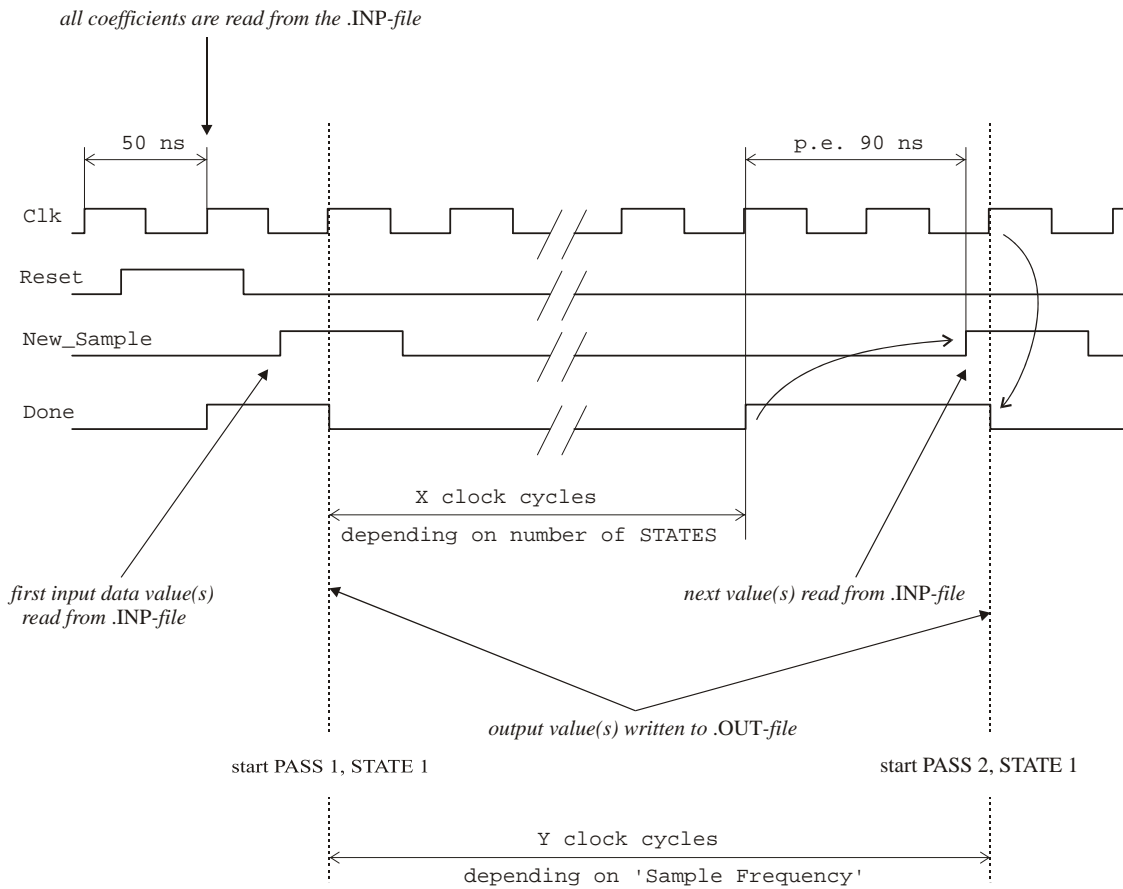
comment lines are allowed before the coefficients block and before the inputs block ( in '--' VHDL format )

input values ( for I0 in this example ) are read one by one, while each of them is followed by one pass through the SSG and result in an output value ( from O5 ) in 'FIR5.OUT'

The hex values above hold true for a [17 15] signed 2's complement fixed-point format, e.g. 2 bits for the integer part (of which the MSB reflects the weighted sign-bit) and 15 bits for the fractional part. So x"08000" means 0\_1.000\_0000\_0000\_0000, which is a '1' (unit step function as an input, starting at  $n = 2$ ). It will be clear that x"1F654" (the first and last coefficients) represents a negative number since its sign bit is set.

In the .OUT-file, the same hex format will be used. Output is also written line by line, e.g. one data line for each output resulting from the same input sample, then the same procedure for the next sample, and so on. The .OUT-files are started with two comment lines, which a.o. lists the format in which the hex data has been written.

## Simulation timing setup



The simulation starts each run with an initialization phase in which an asynchronous Reset is issued that clears all internal registers. At the first positive going edge of the (SSG/system) Clk when Reset is high, all coefficients from the .INP-file are read and the Done bit goes high to signal that the SSG is ready and awaiting.

At each New\_Sample (= Start) going high, a new input data value (or as many input values as there are external inputs) is (are) read from the .INP-file. At the first positive going edge of the clock, the SSG process sets Done low and starts with its first STATE. The STATES are advanced each clock period. Finally, its Done signal goes high again, and everything is halted until the next sample arrives. When this actually happens is, of course, determined by the sample frequency to SSG clock ratio and, when the sample frequency is relatively low, can take a large number of SSG clock cycles. In the simulation testbench, the time that a new sample pulse trails the Done edge is fixed and set to a value of 90 ns, slightly less than 2 clock periods (one Clk-period is set to 50 ns).

The .OUT-file is written each time that Done goes low with the same number of output values as there are external output ports.

## Overview of the Software Environment

Both `gen_mTB` and `gen_VHD` will write a number of files in specific directories that will be created automatically when the programs are used for the first time.

Suppose that you are working with a `.cir`-file called 'NAME.cir' and that you saved this file in the directory '\$YOUR\_CIR\_DIR', then

after running `gen_mTB` a new directory will be created, with the following files:

```
<$YOUR_CIR_DIR>/NAME/matlab / testbench_NAME_auto.m  
                             TB_NAME_auto.m  
                             NAME.INP ←
```

this is the m-file you will call

`gen_VHD_template` will result in the following set-up:

```
<$YOUR_CIR_DIR>/NAME/vhdl / testbench_NAME_auto.vhd  
                             NAME_auto.vhd  
                             NAME_SSG_auto.vhd  
                             resources_reg.vhd  
                             txt_util12.vhd  
                             NAME.INP ←
```

all 6 files are needed for simulation

create these .INP-files  
(they can be identical)

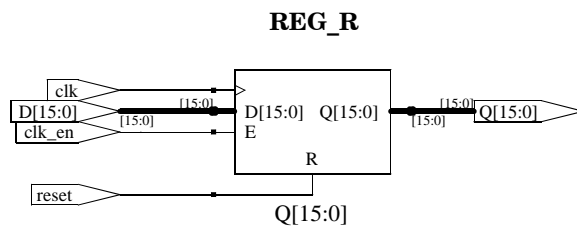
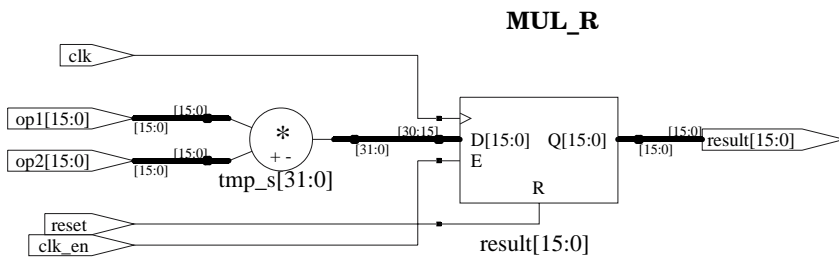
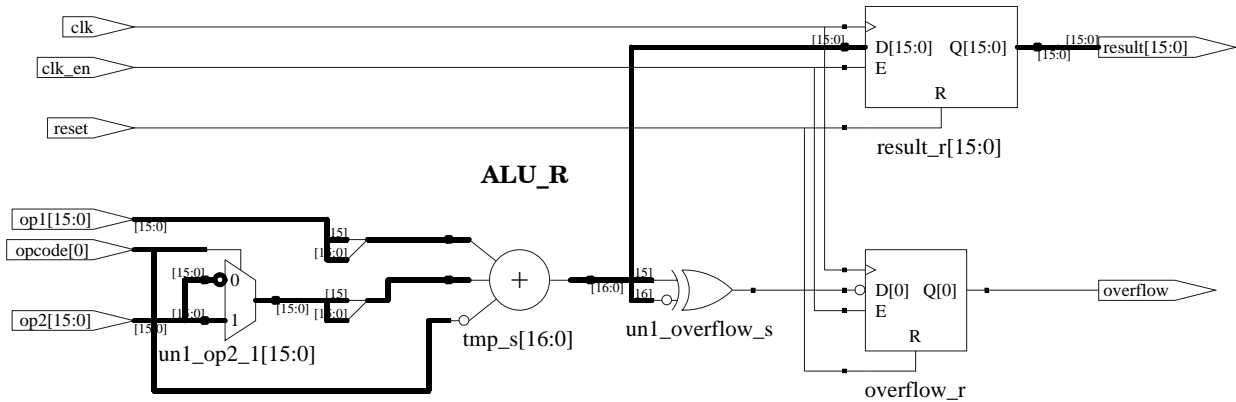
these 3 files are needed for synthesis

Both testbenches will write a file `NAME.OUT` in the directory from where they are run.



## VHDL resources

If synthesized with Synplify Pro, the architectures described in resources\_reg.vhd with their generic buswidths [17 15], viz. ALU\_R, MUL\_R and REG\_R, look as shown below.



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